CLAIMS

What is claimed is:

1. A method of configuring a programmable logic device including non-volatile and volatile memories, the non-volatile memory including a plurality of words comprising configuration data for the programmable logic device, each word including a first transfer bit having a first stored value that is one of a "programmed" value and an "erased" value, the method comprising:

powering up the programmable logic device;

repeating the following sequence for a series of the words in the non-volatile memory, from a first word to a final word:

transferring one of the words from the non-volatile memory to the volatile memory, and

detecting a first detected value of the first transfer bit transferred from the non-volatile memory to the volatile memory; and

repeating, if the first detected value is different from the first stored value for any one word, transferring the first word from the non-volatile memory to the volatile memory.

2. The method of Claim 1, further comprising:

beginning operation of the programmable logic device after the final word is transferred and detected, if the first detected value for each word is the same as the first stored value for the same word.

3. The method of Claim 1, further comprising:

storing the plurality of words in the non-volatile memory prior to powering up the programmable logic device.

4. The method of Claim 1, wherein the first transfer bit is in the same location of each word.

5. The method of Claim 1, wherein each word further includes a second transfer bit having a second stored value, the second stored value being different from the first stored value.

6. The method of Claim 5, further comprising:

for each transferred word, detecting a second detected value of the second transfer bit transferred from the non-volatile memory to the volatile memory; and

repeating, if the second detected value is different from the second stored value for any one word, transferring the first word from the non-volatile memory to the volatile memory.

7. The method of Claim 1, further comprising:

setting a latch to a predetermined initialization value while powering up the programmable logic device; and

for each transferred word, changing a value in the latch from the predetermined initialization value, if the first detected value is different from the first stored value.

8. The method of Claim 1, wherein the programmable logic device is a CPLD.

9. The method of Claim 1, wherein repeating transferring the first word is performed only after transferring the final word.

10. The method of Claim 1, wherein repeating transferring the first word is performed after detecting a first detected value and before transferring the final word.

11. An initialization circuit, comprising:

a non-volatile memory including a plurality of words, each word including a first transfer bit having a first stored value that is one of a "programmed" value and an "erased value", the non-volatile memory having an input port, an output port, and a control input port;

a sensing array having an input port coupled to the output port of the non-volatile memory and an output port, the output port including a first terminal on which a sensed first transfer bit is placed;

a volatile memory having an input port coupled to the output port of the sensing array and a control input port; and

a control circuit coupled to the first terminal of the sensing array and the control input ports of the non-volatile and volatile memories.

12. The initialization circuit of Claim 11, wherein the first transfer bit is in the same location of each word.

13. The initialization circuit of Claim 11, wherein:

each word further includes a second transfer bit having a second stored value, the second stored value being different from the first stored value;

the sensing array output port further includes a second terminal on which a sensed second transfer bit is placed; and

the control circuit is further coupled to the second terminal of the sensing array.

14. The initialization circuit of Claim 11, wherein the control circuit comprises a latch coupled to the first terminal of the sensing array.

15. The initialization circuit of Claim 11, wherein the initialization circuit comprises a portion of a programmable logic device.

16. The initialization circuit of Claim 15, wherein the plurality of words comprises configuration data for the programmable logic device.

17. The initialization circuit of Claim 15, wherein the programmable logic device is a CPLD.

18. An apparatus for configuring a programmable logic device including non-volatile and volatile memories, the non-volatile memory including a plurality of words comprising configuration data for the programmable logic device, each word including a first transfer bit having a first stored value that is one of a "programmed" value and an "erased" value, the apparatus comprising:

means for powering up the programmable logic device;

means for transferring each of the words from the non-volatile memory to the volatile memory, in a sequence of words from a first word to a final word;

means for detecting for each word a first detected value of the first transfer bit transferred from the non-volatile memory to the volatile memory; and

means for repeating, if the first detected value is different from the first stored value for any one word, transferring each of the words from the non-volatile memory to the volatile memory and detecting for each word a first detected value.

19. A method of transferring data from a non-volatile memory to a volatile memory in a circuit, the non-volatile memory including a plurality of words, each word including a first transfer bit having a first stored value that is one of a "programmed" value and an "erased" value, the method comprising:

powering up the circuit;

repeating the following sequence in response to the powering up the circuit, for a series of the words in the non-volatile memory, from a first word to a final word:

transferring one of the words from the non-volatile memory to the volatile memory, and

detecting a first detected value of the first transfer bit transferred from the non-volatile memory to the volatile memory; and

repeating, if the first detected value is different from the first stored value for any one word, transferring the first word from the non-volatile memory to the volatile memory.

20. The method of Claim 19, further comprising:

beginning operation of the circuit after the final word is transferred and detected, if the first detected value for each word is the same as the first stored value for the same word.

21. The method of Claim 19, further comprising:

storing the plurality of words in the non-volatile memory prior to powering up the circuit.

22. The method of Claim 19, wherein the first transfer bit is in the same location of each word.

23. The method of Claim 19, wherein each word further includes a second transfer bit having a second stored value, the second stored value being different from the first stored value.

24. The method of Claim 23, further comprising:

for each transferred word, detecting a second detected value of the second transfer bit transferred from the non-volatile memory to the volatile memory; and

repeating, if the second detected value is different from the second stored value for any one word, transferring the first word from the non-volatile memory to the volatile memory.

25. The method of Claim 19, further comprising:

setting a latch to a predetermined initialization value while powering up the circuit; and

for each transferred word, changing a value in the latch from the predetermined initialization value, if the first detected value is different from the first stored value.

26. The method of Claim 19, wherein the circuit is an integrated circuit (IC).

27. The method of Claim 19, wherein the circuit is a programmable logic device.

28. The method of Claim 19, wherein the programmable logic device is a CPLD.

29. The method of Claim 19, wherein repeating transferring the first word is performed only after transferring the final word.

30. The method of Claim 19, wherein repeating transferring the first word is performed after detecting a first detected value and before transferring the final word.

31. An apparatus for transferring data from a non-volatile memory to a volatile memory in a circuit, the non-volatile memory including a plurality of words, each word including a first transfer bit having a first stored value that is one of a "programmed" value and an "erased" value, the apparatus comprising:

means for powering up the circuit;

means for transferring each of the words from the non-volatile memory to the volatile memory, in a sequence of words from a first word to a final word;

means for detecting for each word a first detected value of the first transfer bit transferred from the non-volatile memory to the volatile memory; and

means for repeating, if the first detected value is different from the first stored value for any one word, transferring each of the words from the non-volatile memory to the volatile memory and detecting for each word a first detected value.